

**256Kx4 Monolithic  
CMOS Static RAM  
Commercial and Military**

PRELIMINARY

**Features**

The EDI84256CS/LPS/PS is a high speed, high performance, megabit density monolithic Static RAM organized as 256Kx4 bits for both commercial and military applications.

Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

Military product compliant to MIL-STD-883, Paragraph 1.2.1 is available.

Two low power versions are available, PS and LPS, for Military products. The LPS version includes a 2V Data Retention Function for battery back-up operation.

256Kx4 bit CMOS Static  
Random Access Memory

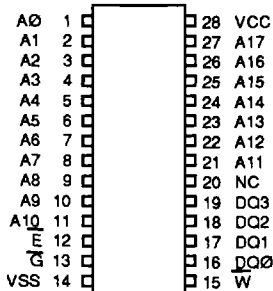
- Fast Access Times  
Commercial: 20, 25, and 35ns  
Military: 25, 35, 45, and 55ns
- $\bar{E}$  and  $\bar{G}$  Functions for Bus Control
- TTL Compatible I/O
- Common Data Inputs and Outputs
- Fully Static, No Clocks

Thru-hole and Surface Mount Package Options

- 28 Pin Dual-in-line Packages, JEDEC Pinout  
Ceramic DIP, 400 mils Wide, No. 101  
Plastic DIP, 400 mils Wide, No. 13
- 28 Lead Plastic SOJ, No. 22
- 28 Pad Ceramic LCC, No.76
- 28 Lead Ceramic SOJ, No. 77
- 28 Lead Ceramic Flatpack, No. 79

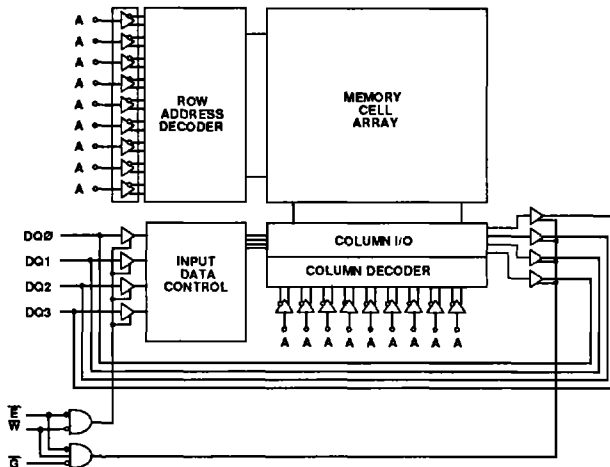
Single +5V ( $\pm 10\%$ ) Supply Operation

**Pin Configuration  
and Block Diagram**



**Pin Names**

- |           |                          |
|-----------|--------------------------|
| A0-A17    | Address Inputs           |
| $\bar{E}$ | Chip Enable              |
| $\bar{W}$ | Write Enable             |
| $\bar{G}$ | Output Enable            |
| DQ0-DQ3   | Common Data Input/Output |
| VCC       | Power (+5V $\pm 10\%$ )  |
| VSS       | Ground                   |
| NC        | No Connection            |



### Absolute Maximum Ratings\*

Voltage on any pin relative to VSS .....	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial .....	0°C to +70°C
Industrial .....	-40°C to +85°C
Military .....	-55°C to +125°C
Storage Temperature	
Plastic .....	-55°C to +125°C
Ceramic .....	-65°C to +150°C
Power Dissipation .....	1 Watt
Output Current .....	20 mA
Junction Temperature, T <sub>J</sub> .....	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

### AC Test Conditions

Input Pulse Levels .....	VSS to 3.0V
Input Rise and Fall Times .....	5ns
Input and Output Timing Levels .....	1.5V
Output Load .....	1TTL, CL = 30pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

### DC Electrical Characteristics

Parameter	Sym	Conditions	Temp Range	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}, E = VIL, I/O = 0mA, \text{Min Cycle}$			80	150	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq VIH, VIL \geq VIN \geq VIH$				30	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq VCC-0.2V$ $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$	CS		1	10	mA
			LPS/PS		--	5	mA
Input Leakage Current	ILI	$VIN = 0V \text{ to } VCC$			--	±5	µA
Output Leakage Current	ILO	$V I/O = 0V \text{ to } VCC$			--	±10	µA
Output High Voltage	VOH	$IOH = -4.0mA$		2.4			V
Output Low Voltage	VOL	$IOL = 8.0mA$				0.4	V

### Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

### Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC Plastic DIP SOJ	Ceramic FP/DIP CSOJ	
Input (Except DQ Pins)	CI	6	12	pF
Control (DQ Pins)	CD/Q	8	14	pF

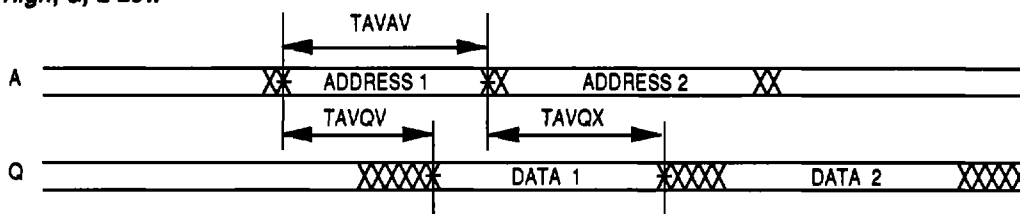
These parameters are sampled, not 100% tested.

## AC Characteristics

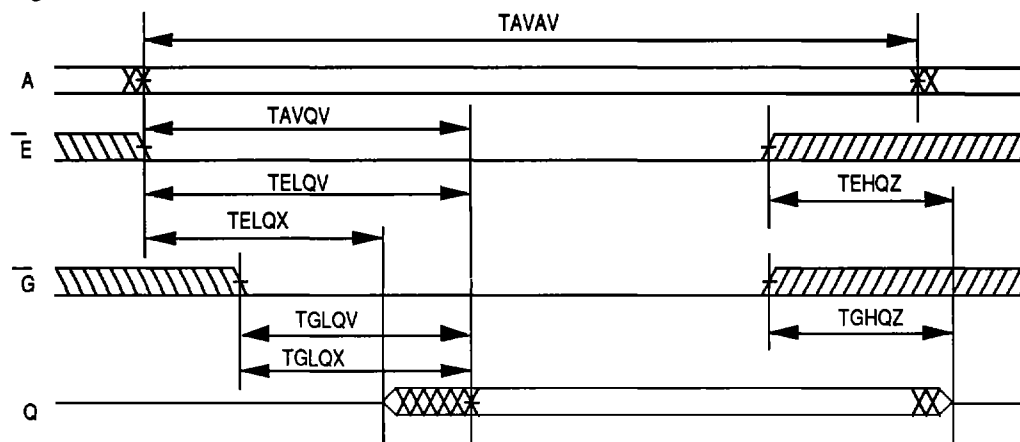
### Read Cycle

Parameter	Symbol	20ns		25ns		35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	20		25		35		45		55		ns
Address Access Time	TAVQV		20		25		35		45		55	ns
Chip Enable Access Time	TELQV		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ		10		12		20		25		25	ns
Output Hold from Address Change	TAVQX	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV		8		10		20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ		8		10		20		25		25	ns

#### Read Cycle 1 W High; G, E Low



#### Read Cycle 2 W High

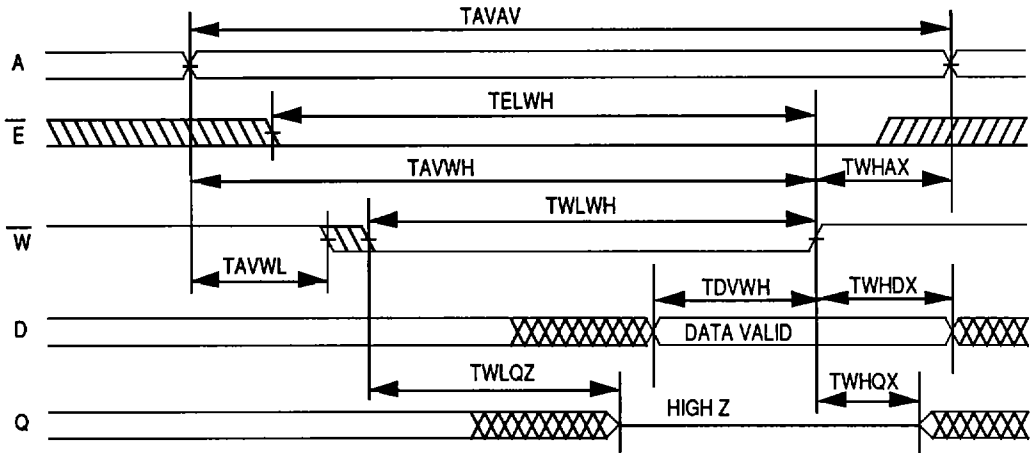


**AC Characteristics**  
**Write Cycle**

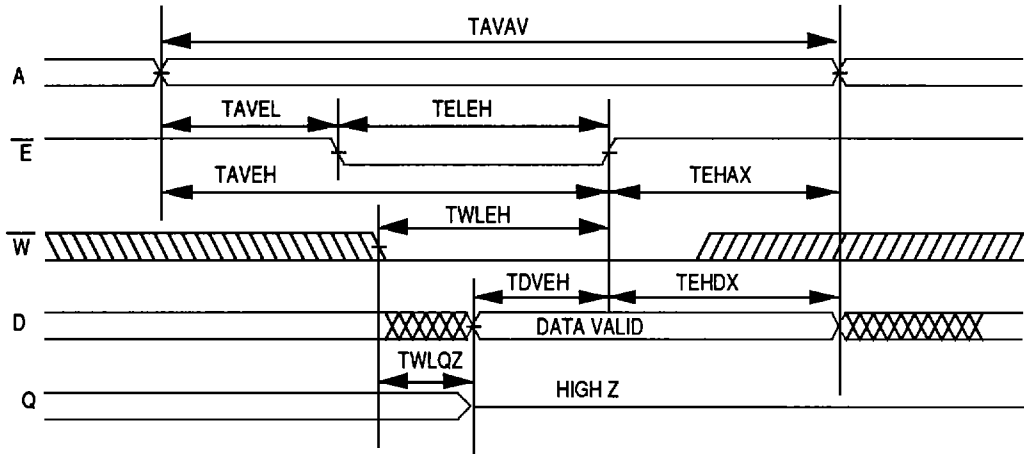
Parameter	Symbol	20ns		25ns		35ns		45ns		55ns		Units	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	TAVAV	20		25		35		45		55		ns	
Chip Enable to	TELWH	$\overline{W}$	15		20		30		35		40		ns
End of Write	TWLEH	$\overline{E}$	15		20		30		35		40		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	15		20		30		35		40		ns
End of Write	TAVEH	$\overline{E}$	15		20		30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	15		20		30		35		40		ns
	TELEH	$\overline{E}$	15		20		30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	8	0	10	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	12		15		20		25		25		ns
	TDVEH	$\overline{E}$	12		15		20		25		25		ns
Output Active from End of Write (1)	TWHQX		3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

**Write Cycle 1**  
**W Controlled**



**Write Cycle 2**  
 **$\bar{E}$  Controlled**



### Data Retention Characteristics

Low Power (LPS) Version Only

(TA = -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\bar{E} \geq VDD - 0.2V$	--	0.750	2	mA
Chip Disable to Data Retention Time	TCDR	VIN $\geq$ VDD - 0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN $\leq$ 0.2V	TAVAV*		--	ns

\*Read Cycle Time

### Data Retention E Controlled

